

THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 27

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte OLE K. NILSSEN

Appeal No. 1996-1664
Application No. 08/272,647¹

ON BRIEF

Before HAIRSTON, KRASS, and BARRETT, Administrative Patent Judges.

HAIRSTON, Administrative Patent Judge.

DECISION ON APPEAL

¹ Application for patent filed July 11, 1994. According to appellants, the application is a continuation of Application No. 07/820,918, filed January 15, 1992, now abandoned, which is a continuation-in-part of Application No. 07/281,275, filed December 7, 1988, now abandoned, which is a continuation-in-part of Application No. 07/080,865, filed August 3, 1987, now U.S. Patent No. 4,819,146, issued April 4, 1989.

This is an appeal from the final rejection of claims 32 through 34.

The disclosed invention relates to a circuit arrangement that alters the output voltage of an inverter circuit.

Claims 32 and 33 are illustrative of the claimed invention, and they read as follows:

32. An arrangement comprising:

a source operative to provide a substantially constant magnitude DC voltage at a pair of DC terminals;

an inverter circuit assembly connected with the DC terminals and operative to provide an AC output voltage at a pair of inverter terminals; the AC output voltage being a voltage that alternates in an periodic manner between a first substantially fixed voltage level and a second substantially fixed voltage level, spending a first time period at the first voltage level and a second time period at the second voltage level; the inverter output voltage consisting of repeated cycles; each cycle having a total cycle period; the sum of the first and second time periods equaling the total cycle period; the inverter circuit assembly including control means operative to control the RMS magnitude of the AC output voltage;

gas discharge lamp having a pair of lamp terminals; and

coupling circuit assembly connected between the inverter terminals and the lamp terminals.

33. An arrangement comprising:

a source operative to provide a DC voltage at a pair of DC terminals;

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an inverter circuit assembly connected with the DC terminals and operative to provide an inverter output voltage at a pair of inverter terminals; the inverter output voltage being a voltage that alternates in an periodic manner between a first substantially fixed voltage level and a second substantially fixed voltage level, spending a first time period at the first voltage level and a second time period at the second voltage level; the duration of the first period being substantially different from the duration of the second period; the inverter output voltage consisting of repeating cycles; each cycle having a total cycle period; the sum of the first and second time periods equaling the total cycle period; the inverter means being further characterized by including a control circuit operative to control the ratio between the duration of the first period and that of the second period;
gas discharge lamp having a pair of lamp terminals; and

coupling circuit assembly connected between the inverter terminals and the lamp terminals.

The reference relied on by the examiner is:

Quazi et al. (Quazi) 4,933,605 June 12,
1990

Claims 32 through 34 stand rejected under 35 U.S.C. § 103
as being unpatentable over Quazi.

BACKGROUND

In a March 31, 1994 decision in the parent application,
the Board stated (Decision, pages 3 and 4) that:

The reference to Quazi discloses a circuit arrangement that includes an inverter circuit that produces a high-frequency output for powering a fluorescent lamp via a coupling circuit. Prior art Figure 2 shows an inverter output voltage that

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alternates in a periodic manner between a first substantially fixed voltage level, and a second substantially fixed voltage level. This same Figure clearly shows that: the first voltage level is at that level for a first time period; the second voltage level is at that level for a second time period; the duration of the first period is substantially different from the duration of the second period; the output voltage consists of repeating cycles; the sum of the first and second time periods equals the total cycle period; and that each cycle has a total cycle period.

Appellant's argument that Quazi does not disclose a non-symmetrical voltage waveform is not commensurate in scope with the claimed invention. Nothing in exemplary claim 31 states that each voltage waveform spends more time "on one side of the zero line than on the other side of the zero line." The frame of reference in claim 31 for the inverter output voltage levels is a time line, and not a zero line

In a February 9, 1996 decision in the grandparent application, the Board stated inter alia that "a variation in the magnitude of the AC voltage . . . occurs in . . . Quazi as a result of the pulse-width modulation of the above-noted signals" (Decision, page 9), and that "[s]uch a voltage decrease with changing duration of signal levels appears to us to be consistent with the teachings of . . . Quazi as to dimming control by pulse-width modulating the inverter output

that feeds a series resonant LC circuit" (Decision, pages 9 and 10).

OPINION

The obviousness rejection of claim 32 through 34 is sustained in view of the rationale set forth in the Board's decision in the parent application, and the pulse-width modulation teachings of Quazi discussed in the Board's decision in the grandparent application.

According to Quazi, the control circuit C1 (Figures 8 and 9) "varies the duty cycle of the control pulses occurring at outputs A and B to thus effect dimming or the control of the light intensity" (column 6, lines 50 through 53). "By varying the pulse width, the pulse repetition frequency remains unchanged and thus matched to the resonant frequency of the series resonant circuit" (column 6, lines 53 through 56).

The two broadly claimed time periods in claim 32 could be the same, and the two broadly claimed voltage levels in claim 32 could be the same as well. Claim 32 does not, therefore, have any support for the argument concerning a voltage "spending more time at the first level than at the second level" (Brief, page 3). In any event, the claimed time

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periods and voltage levels in this claim read directly on Figure 2 in Quazi.

With respect to the duration of one time period being "substantially different" (claim 33) or "significant longer" (claim 34) than the duration of the other time period, we are still of the opinion that the control circuit and pulse-width variation teachings of Quazi would have suggested the claimed time periods, especially for dimming control (Brief, pages 3 and 5).

Appellant's argument (Brief, page 4) that the output voltage disclosed in Figure 2 of Quazi shows "a significant component of unidirectional voltage" is inconsistent with the remainder of the disclosure in Quazi.

DECISION

The decision of the examiner rejecting claims 32 through 34 under 35 U.S.C. § 103 is affirmed.

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No time period for taking any subsequent action in
connection with this appeal may be extended under 37 C.F.R.
§ 1.136(a).

AFFIRMED

KENNETH W. HAIRSTON)	
Administrative Patent Judge)	
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)	BOARD OF PATENT
ERROL A. KRASS)	APPEALS
Administrative Patent Judge)	AND
)	INTERFERENCES
)	
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LEE E. BARRETT)	
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Appeal No. 1996-1664
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Appeal No. 96-1664

Application No. 08/272, 647

APJ HAIRSTON

APJ BARRETT

APJ KRASS

DECISION: AFFIRMED

Send Reference(s): Yes No
or Translation (s)

Panel Change: Yes No

Index Sheet-2901 Rejection(s): _____

Prepared: October 10, 2000

Draft Final

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OB/HD GAU

PALM / ACTS 2 / BOOK
DISK (FOIA) / REPORT